MINUET™ -
HARDWARE INTERFACE MANUAL

MIL-STD-1553 BUS CONTROLLER, REMOTE TERMINAL AND BUS MONITOR
SW DRIVER COMPATIBLE WITH DDC® ENHANCED MINIACE®

USER'S MANUAL FOR:
MNT1553PCI-8 & MNT1553LB-16

Rev 1.01

July 2011

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1 INTRODUCTION

1.1 ABOUT THIS MANUAL

This document is the user's manual for MINUET™ devices MNT1553PCI-8 and MNT1553LB-16 family. These components are Mil-Std-1553 terminals, and are software compatible to DDC® Enhanced MiniACE® .

This manual describes the hardware interface to the MINUET™ components.

The MNT1553PCI-8 device is an 8mm square Mil-Std-1553 component, supporting all three modes of operation – Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (MT), with 8k Words of memory and 33/66MHz PCI bus interface.

The MNT1553LB-16 device is a 17mm square Mil-Std-1553 component, supporting BC, RT and MT modes with 16k Words of memory and Local Bus interface. This component supports various clock frequencies.

In order to reduce the complexity of this manual, it is split from the Software Interface Manual. The Software Interface Manual describes all software modes, registers access and memory management of the components. A high level driver and API documentation is also available as part of the MINUET™ software package.

In order to communicate on a 1553 bus, all MINUET™ components require the use of a 1553 transceiver and transformer. The interface with a 1553 transceiver is covered by this manual on chapter 0.

Depending on model, MINUET™ components communicate with the local host by either PCI bus or a Local Bus. The PCI interface is covered on chapter 4.4 and Local Bus interface is covered on chapter 4.3.

Chapter 3 covers the electrical characteristics of MINUET™ components.

Chapter 7 discusses the design considerations when implementing a board that uses MINUET™ components.

Note:
Please note that it is assumed that the user of this manual is knowledgeable about the DDC MiniACE and Enhanced MiniACE components, and their software interface. It is also assumed that the user of this manual has knowledge of Mil-Std-1553 protocol.

1.2 ABOUT MINUET™

1.2.1 GENERAL DESCRIPTION

The MINUET™ family of Mil-Std-1553 devices integrate Mil-Std-1553B protocol engine, memory management, processor or PCI interface logic, and 8K or 16K words of RAM in a 8mm or 17mm square package.

The MINUET™ devices are software compatible to DDC® BU-XXXXX devices. A system designed to operate with any of the DDC® ACE, Mini-ACE®, Enhanced Mini-ACE® or Micro-ACE® components can work seamlessly with MINUET™ component without software changes.

In addition, Sital offers a software package, which includes device drivers, advanced programming interface (API) and test applications for carious operating systems. Sital's software package, at API level, is also compatible to the DDC® API.

The MINUET™ components were validated to meet the MIL-STD-1553B Notice 2 Remote Terminal Validation test plan, thus reliving the user from mastering the standard.

A MINUET™ device is able to work in conjunction with any standard 1553 transceiver, or with Sital's discrete transceiver. A complete 1553 solution includes an 8mm MINUET™ component, a 1553 transceiver and 2 transformer components.

MINUET™ is available in several configurations:

- 8mm sqr, BC/RT/MT, 8K Words of internal RAM and local bus interface.
- 8mm sqr, BC/RT/MT, 8K Words of internal RAM and PCI interface.
- 17mm sqr, BC/RT/MT, 16K Words of internal RAM and local bus interface.
- 17mm sqr, BC/RT/MT, 16K Words of internal RAM and PCI interface.

MINUET™ offers several benefits over existing Mil-Std-1553 components, including very small size, flexible interface, low power consumption, flexible clock frequency and compatibility to existing software drivers and applications.

The approach offered by Sital, to separate the 1553 protocol interface from the 1553 analog front-end, enable users for better flexibility when designing the system or layout the PCB. For example – the MINUET™ component can be physically located near the PCI connector, while the 1553 transceiver and transformer can be near the 1553 connector. The signals in between MINUET™ and 1553 transceiver are less sensitive to Signal Integrity issues than PCI signals or 1553 analog signals.

Sital provides several tools for better use of MINUET™, including the MINUET™ evaluation board (BRD1553PCI) and the Luthier™ software tool for managing 1553 communications bus via MINUET™ devices.

All MINUET™ components work at industrial temperature range of -40C to +85C.

1.2.2 BACK-END INTERFACE

The MINUET™ family offers two separate ways of back-end interface – PCI and Local Bus.

The Local Bus interface contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus.

The PCI interface is a standard PCI "Target" interface compliant with PCI 2.2 standard.

The memory management scheme for RT mode provides three data structures for buffering incoming and outgoing data. Combined with the MINUET's extensive interrupt capability, these structures serve to ensure data consistency while off-loading the host processor. The MINUET™ devices can optionally boot-up as a RT with the "Busy" bit set for 1760 applications. The MINUET™ BC mode implements several features aimed at providing an efficient real-time software interface to the host processor including automatic retries, programmable inter-message gap times or message rate, automatic frame repetition, and flexible interrupt generation.

1.2.3 INTERFACE TO THE 1553 BUS

The MINUET™ components require external 1553 Transceiver and a coupling transformer.

MINUET™ can work with any existing 1553 transceiver, or with Sital's Discrete components transceiver design.

For example, together with National Hybrid's (NHI) BUS+, Transceiver and Transformer packed together, this is the smallest available total solution for 1553 bus. Any Holt or NHi 7mm dual transceiver or DDC single transceiver can also be used for space saving purposes.

A "Transceiver_Select" pin is used to select between a standard transceiver and Sital's Discrete transceiver.

1.2.4 PRODUCTS SELECTION

The following table shows the different models of MINUET™ and the functionality:

Device Number	Package	1553 Functionality	Backend Interface	Clock Frequency	RAM (16 bits)
MNT1553PCI-8	8mm X 8mm, 132-Ball csBGA	BC/RT/MT	PCI	33/66 MHz	8K RAM
MNT1553PCI-16	17mm X 17mm 256-Ball ftBGA	BC/RT/MT	PCI	33/66 MHz	16K RAM
MNT1553LB-8	8mm X 8mm, 132-Ball csBGA	BC/RT/MT	Local Bus	10/12/16/20/ 24/32/40 MHz	8K RAM
MNT1553PCI-16	17mm X 17mm 256-Ball ftBGA	BC/RT/MT	Local Bus	10/12/16/20/ 24/32/40 MHz	16K RAM

1.2.5 MINUET™ KEY FEATURES

- **MIL-STD-1553B Notice 2 Compliant Terminals.**
  - Supports Bus Controller mode or simultaneous Remote Terminal/Monitor mode.
  - Software Compatible to DDC ACE®, Mini-ACE®, Enhanced Mini-ACE® and Micro-ACE® Components.
  - Software drivers used with any DDC® component can be used seamlessly with MINUET™.
  - Provided also with software drivers and API, compatible to DDC® at the API level.
- **Smallest Solution Available - 8x8mm or 17x17mm BGA.**
  - 132-Ball csBGA (8x8 mm) or 256-Ball ftBGA (17 x17 mm) Package.
  - PCI or Local Bus Interface.
  - 33/66MHz PCI bus interface, suitable for connecting directly to PCI bus.
  - Supports PCI burst mode.
  - Simple address/data bus for connecting to local CPU.
- **3.3V and 1.2V operation, very low power consumption.**
- **Operates from wide range of clock frequencies.**
  - 10, 12, 16, 20, 24, 32 and 40MHz available. 33/66MHz for PCI interface.
  - Customer may order specific clock frequency.
- **Flexible pinout configuration for easy PCB Layout.**
  - Customer may order different pinout configurations.
- **Very fast access 8K x 16 or 16K x 16 bits Shared RAM.**
  - True dual-port RAM for fast access to the device from CPU or PCI bus.
  - The 8mm package comes with 8K words of shared RAM and the 17mm package comes with 16K words of shared RAM.
  - Access to RAM can be synchronized to PCI or local bus clock, enabling burst read/write.
- **Bootable RT option required for MIL-STD-1760.**
  - Supports 'Busy' bit at status word during CPU boot.
  - RT Address is set by discrete bits.
- **PCI Evaluation board available – BRD1553PCI.**
- **Provided with Luthier™ - software tool for 1553 bus operation.**

1.3 TERMS USED IN THIS DOCUMENT

- Remote Terminal (RT) – The part of the FPGA that manages the 1553 communications and implemented by the core.
- SubSystem – The whole box that connects to the MIL-STD-1553 bus that contains the FPGA – part of it is the Remote Terminal.
- Host – the CPU running the SubSystem and managing the device interface.
- FPGA – Programmable device that contains the 1553 core and user logic and is part of the Subsystem.
- 1553 Core – Supplied logic circuit that interfaces to MIL-STD-1553 bus.
- ICD - Interface Control Document.
- BC – Bus controller.
- TA – Terminal Address of the command / status words. Bits 11 to 15.
- SA – Sub Address of the command word. Bits 5 to 9.
- WC – Word count field of command. Bits 0 to 4.
- Muxbus – Time multiplexed bus known as the MIL-STD-1553B Notice 2 bus.
- SW – software.
- BCST – Broadcast command.
- TX – Transmit.
- RX – Receive.
- SACW – The Sub-address control word.
- LUT – Look up Table.

2 ARCHITECTURE OVERVIEW

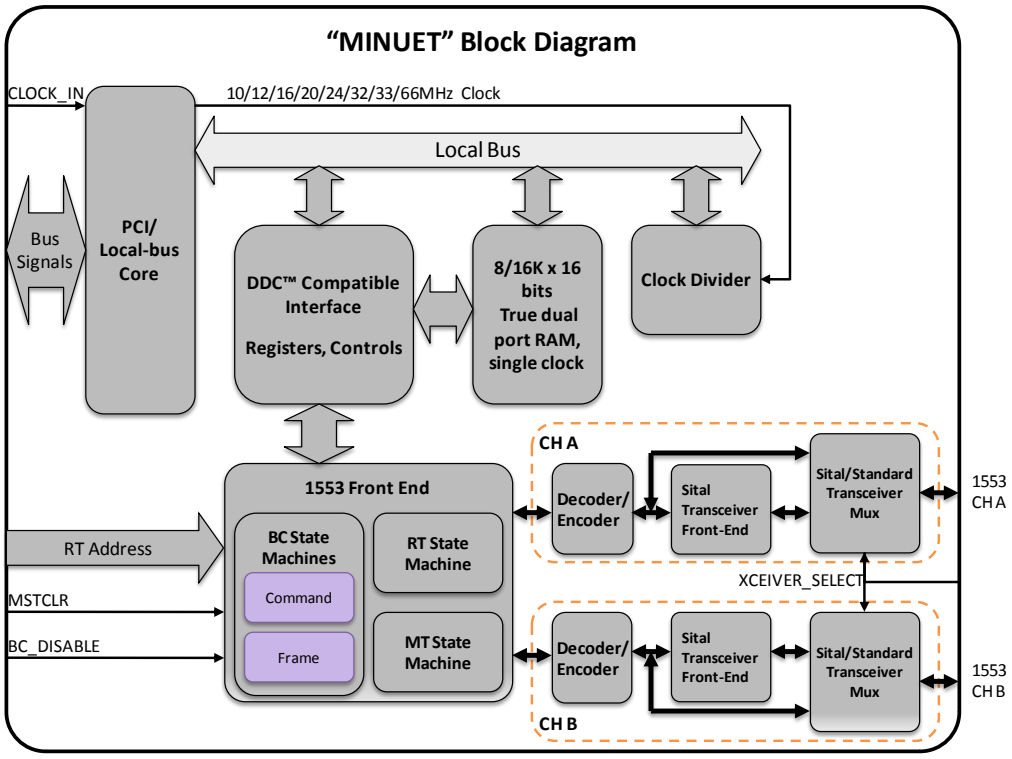


Figure 1: MINUET™ Block Diagram

2.1 1553 FRONT-END

Each MINUET™ device contains a 1553 Front-End core which performs all the functionality of managing the Mil-Std-1553 protocol interface. This core is responsible for producing the messages, commands, responses, and managing the 1553 frames. The core is built of several state machines that follow the Mil-Std-1553B standard. There are separated state machines for Remote Terminal, Monitor and Bus Controller.

The 1553 Front-End core is controlled be the configuration registers at the DDC® Compatible Interface block. RT Address pins are connected directly to the 1553 Front-End so that in case of 1760 protocol requirement the core will respond with a "Busy" bit to any request from the 1553 bus, even before the control registers and memory are configured by the host CPU.

A MSTCLR (Master Clear) input is used for resetting all state-machines.

The BC_DISABLE input can be used in case a design requires Remote Terminal or Monitor operation only. In such case this input will prevent any option of accidently configuring the device as Bus Controller.

2.1.1 THE RT STATE MACHINE

The RT state machine constantly listens to the bus activity and identifies a set of bus words as a valid message, being 'transmit', 'receive', 'mode' or 'broadcast' message, and acts accordingly.

Data messages being received from the bus are saved into the dual-port RAM via the DDC® compatible interface block as they arrive. Messages that need to be transmitted to the bus are fetched from the dual-port RAM via the DDC® compatible interface block, as they are being transmitted to the bus.

Errors, channel status and other information on the 1553 communications status is reported to the DDC® compatible interface block, and reflected to the software at the control registers and memory.

2.1.2 THE MONITOR STATE MACHINE

The Monitor state machine searches for valid commands. When a command is found, the state machine checks whether this command defines a message required for monitoring. In such case, the state machine manages the process of storing the words one by one in the Dual-Port memory via the DDC® compatible interface block into a pre-defined location.

2.1.3 BC STATE MACHINE

When transmission is initiated the frame state machine manages the sequencing of a whole frame of messages as defined by the configuration registers and fixed memory locations in the memory. The frame is composed of a set of individual messages being transmitted and managed over the 1553 bus one after the other. The host also points the beginning of the first message in memory and defines how many messages to transact through 2 fixed location memory words. When all data has been loaded, and the state machines are idle, the host sends a START command. As a response, the frame state machine starts the frame transmission. The frame state machine fetches the messages from memory and forwards the requested message information to the command state machine which in turn sequences the command data and status words for a complete legal 1553 message. When the message is complete the frame state machine accesses the next command, and so on until all messages have been completed.

The command state machine either transmits words through the encoders or receives RT responses through the decoders. The encoders and decoders interface between the core's 16 bits parallel internal buses and the MuxBus serial bus.

2.2 DECODER/ENCODERS

The Front-End core is connected to two separate Decoder/Encoders, one for each dual-redundant 1553 channel. The Decoder/Encoder blocks translate the serial bus messages from the MIL-STD-1553 Manchester coding and format, into a 16 bit parallel data accompanied by status indications for each word. These Decoder/Encoders are carefully designed to overcome noise and other problems related to the 1553 bus.

2.3 SITAL TRANSCEIVER FRONT-END

MINUET™ can be connected to any off-the-shelf transceiver or to Sital's discrete transceiver. The Sital transceiver requires some additional control logic, which is managed by the Sital Transceiver Front-End cores. These cores perform signal shaping, filtering and short-circuit protection for the Sital analog Front-End.

Users can select between the Sital discrete transceiver and the standard transceiver via the XCEIVER_SELECT input pin, which controls the multiplexer between the Sital Transceiver Front-End core and the standard interface directly from the Decoder/Encoder.

2.4 DDC® COMPATIBLE INTERFACE BLOCK

The operation of the 1553 Front-End state machines is controlled by the DDC® Compatible Interface block. This block contains the control registers and memory interface to the dual-port RAM. This block creates the control signals for the 1553 Front-End core. The registers and interface are explained in details in MINUET™ Software Interface Manual.

The interface to the device is divided between several control registers and memory access. The registers are used to control the device and its operation, and the memory is used as the 1553 message interface and control.

The software interface of MINUET™ to the host processor consists of 32 internal operational registers for normal operation. These registers determine the device configuration, modes of operation, memory structure, interrupt control and status, etc.

The registers are mapped to address 0x0 to 0x20 (Hexadecimal) and can be written or read (depending on their functionality). Memory can be 8K or 16K (depending on model) – all by 16 bits.

The data reception and transmission is controlled on a message-by-message basis. Each message is stored in the memory or read from the memory based on mapping defined by the host CPU during offline state. The host CPU sets up the mapping and modes of operations in the dual port RAM and in the configuration registers. The mapping options are discussed in the software manual.

Access to the registers or memory is done through the same address and data lines. When on PCI mode, then memory and registers are mapped to a different base address. When Local-Bus mode, when accessing the registers, the MEM/REG signal (which is one of the bus signals) should be kept low, and when accessing the memory this signal should be high.

There are several dependencies between the configuration of registers and the configuration and operation of the memory. The user must verify that all dependencies configured correctly with accordance to the required operation of the device.

2.5 DUAL-PORT RAM

The True Dual-Port RAM stores messages received or to be transmitted to the 1553 bus. The messages are arranged in memory with accordance to the DDC® Mini-ACE® memory structure and user's configuration.

The memory is a true dual port RAM, with both sides independently reading or writing data. When operating as Local Bus, it is preferred that the Host CPU will supply the memory control signals, address, data, chip select and write enable, synchronized with the clock signal supplied to the core. This synchronized approach will ensure robustness of operation. Since MINUET™ and the Host CPU work with the same clock, the design will have no transient effects. Therefore, MINUET™ enables a wide selection of clock frequencies.

When operating as PCI interface, MINUET™ uses the PCI clock of 33MHz or 66MHz.

2.6 PCI/LOCAL BUS INTERFACE

Selection between PCI or Local Bus interface is depending on MINUET™ model. When PCI interface, the PCI IP core bridges between a 32 bit, 33Mhz or 66Mhz PCI bus and internal local bus.

3 HARDWARE CHARACTERISTICS

3.1 DC AND SWITCHING CHARACTERISTICS

3.1.1 ABSOLUTE MAXIMUM RATINGS [1, 2]

Supply Voltage VCC . . . . . -0.5 to 1.32V
Output Supply Voltage VCCIO . . . . . -0.5 to 3.75V
Input or I/O Tristate Voltage Applied[3] . . . . . -0.5 to 3.75V
Storage Temperature (Ambient) . . . . . -65 to 150°C
Operating Temperature . . . . . -40°C to +85°C
Junction Temperature Under Bias (Tj) . . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. All voltages referenced to GND.
3. Overshoot and undershoot of -2V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.

3.1.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Units
VCC	Core Supply Voltage	1.14	1.26	V
VCCIO	I/O Driver Supply Voltage	3.135	3.465	V
tJIND	Junction Temperature, Industrial Operation	-40	100	°C

3.1.3 SUPPLY CURRENT AT 25°C

Over Recommended Operating Conditions:

Symbol	Parameter	Device	Typical	Units
ICC	Core Supply Current (1.2V)	MNT1553PCI-8	50	mA
		MNT1553LB-8	50	mA
		MNT1553PCI-16	60	mA
		MNT1553LB-16	60	mA
ICCIO	I/O Driver Supply Current (3.3V)	MNT1553PCI-8	140	mA
		MNT1553LB-8	140	mA
		MNT1553PCI-16	150	mA
		MNT1553LB-16	150	mA

3.1.4 SUPPLY CURRENT AT 85°C

Over Recommended Operating Conditions:

Symbol	Parameter	Device	Max.	Units
ICC	Core Supply Current (1.2V)	MNT1553PCI-8	325	mA
		MNT1553LB-8	325	mA
		MNT1553PCI-16	465	mA
		MNT1553LB-16	465	mA
ICCIO	I/O Driver Supply Current (3.3V)	MNT1553PCI-8	175	mA
		MNT1553LB-8	175	mA
		MNT1553PCI-16	180	mA
		MNT1553LB-16	180	mA

3.1.5 DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions:

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Logic '1' Output Voltage		VCCIO -0.4	-	-	V
VOL	Logic '0' Output Voltage		-	-	0.4	V
VIH	Logic '1' Input Voltage		2.0	-	3.6	V
VIL	Logic '0' Input Voltage		-0.3	-	0.8	V
IIL, IIH[1]	Input or I/O Low Leakage	0 ≤ VIN ≤ VCCIO	-	-	10	µA
		VCCIO ≤ VIN ≤ VIH (MAX)	-	-	150	µA
IPU	I/O Active Pull-up Current	0 ≤ VIN ≤ 0.7 VCCIO	-30	-	-150	µA
IPD	I/O Active Pull-down Current	VIL (MAX) ≤ VIN ≤ VCCIO	30	-	210	µA
IBHLS	Bus Hold Low Sustaining Current	VIN = VIL (MAX)	30	-	-	µA
IBHHS	Bus Hold High Sustaining Current	VIN = 0.7 VCCIO	-30	-	-	µA
IBHLO	Bus Hold Low Overdrive Current	0 ≤ VIN ≤ VCCIO	-	-	210	µA
IBHHO	Bus Hold High Overdrive Current	0 ≤ VIN ≤ VCCIO	-	-	-150	µA
VBHT	Bus Hold Trip Points		VIL (MAX)	-	VIH (MIN)	V
C1	I/O Capacitance[2]	VCCIO = 3.3V, VCC = 1.2V, VIO = 0 to VIH (MAX)	-	8	-	pf
C2	Dedicated Input Capacitance	VCCIO = 3.3V, VCC = 1.2V, VIO = 0 to VIH (MAX)	-	6	-	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active.
2. T_A 25°C, f = 1.0 MHz.

3.2 1553 INTERFACE CHARACTERISTICS

1553 transceiver Interface Bus levels:					
See paragraph 3.1.5, DC Electrical Characteristics					
1553 message timing:					
Completion of CPU Write (BC Start)- to-Start of Next Message			2.5		µS
BC Inter-message Gap		7	9.5		µS
RT Response Time		4		7	µS
BC/RT/MT Response Timeout				25	µS
Transmitter Watchdog Timeout				770	µS

4 MINUET™ INTERFACES

4.1 INTERFACE TO THE 1553 BUS

4.1.1 1553 CONFIGURATION PINS

Some 1553 parameters can be programmed by software or set by hardware.

The following pins are available for setting parameters of the 1553 configuration:

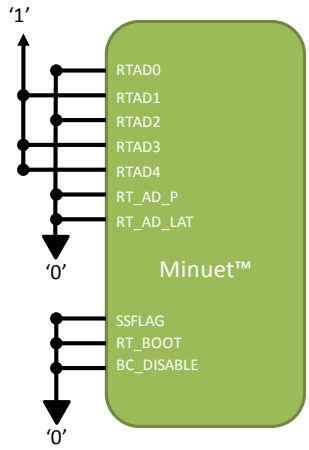
Signal Name	In/Out	Description
SSFLAG/EXT_TRIG	In	RT mode – When low sets the subsystem flag bit in the status word response. BC mode – A rising edge on this signal triggers a frame if external trigger enabled in configuration register #1.
BC_DISABLE	In	When '1' Disables the BC operation. When operating as RT or Monitor only, with no intention of enabling BC mode, then this input should be connected to high.
RTAD0-RTAD4	In	RT address. These pins determine the address of the RT on the 1553 bus.
RT_AD_P	In	RT Address Parity. This pin must create an odd parity sum with RTAD4-0.
RT_AD_LAT	In	RT Address Latch. RT address is latched on rising edge.
RT_BOOT_n	In	When '0' Starts RT Mode in Busy Status. Used for 1760. The RT will respond to any command directed to it with 'Busy', until the RT is initialized by software.
XCEIVER_SELECT	In	Select between Sital and Standard transceiver. When using COTS transceiver then this bit should be tight to '0'. When Sital discrete transceiver, this input should be '1'.

4.1.2 RT ADDRESS CONFIGURATION

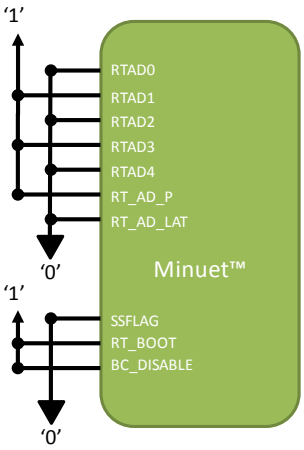
RT Address is configured by the RTAD0 to RTAD4 pins, together with the RT_AD_P and RT_AD_LAT pins.

When RT_AD_LAT is low, then RT Address is determined by RTAD0 – RTAD4 and RT_AD_P. When RT_AD_LAT is high, then the RT address is latched when writing to Configuration Register #5. Therefore, if you wish to set the RT address by software, it is recommended to connect RTAD0 to RTAD4 and RT_AD_P to the data-bus.

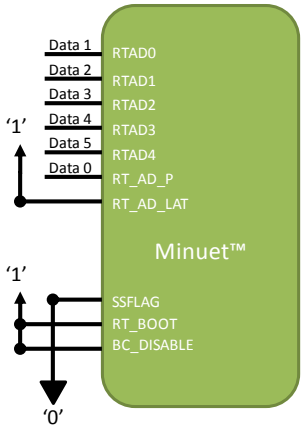
The following drawings show several RT configurations:



1760, RT Address '11010' (RT 26)



1553, RT Address '01010' (RT 10)



RT Address is set by software

4.2 INTERFACE TO 1553 TRANSCEIVERS

The MINUET™ components perform the 1553 digital protocol engine functionality, and therefore require external 1553 Transceiver and a coupling transformer.

MINUET™ can work with any existing off-the-shelf 1553 transceiver, or with Sital's Discrete components transceiver. A "Transceiver_Select" pin is used to select between a standard transceiver and Sital's discrete transceiver.

4.2.1 INTERFACE TO A STANDARD TRANSCEIVER

In case a standard transceiver is used, then each channel should be connected directly from/to MINUET™ in the following manner:

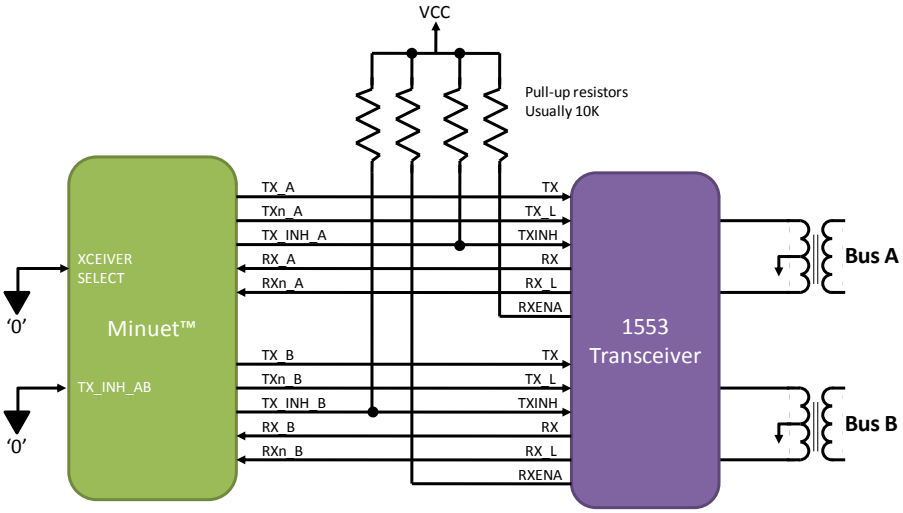


Figure 2: Interface to any off-the-shelf 1553 transceiver

Note that VCC and logic levels must be compatible. Because MINUET™ uses 3.3V interface, then it is required to use a 3.3V transceiver as well. It is always important to verify that the selected transceiver will comply with the logic parameters of MINUET™.

The relevant pins for the 1553 transceiver interface are:

Signal Name	In/Out	Description
TX_INH_AB	In	Transmitter inhibit input for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
TX/TXn-A	Out	Positive and negative polarity of 1553 output signals for Bus A. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-A	In	In phase and negative received signals from transceiver, Bus A.
TX_INH_A	Out	Transmission inhibit signal connected to transceiver. This signal is normally high, and is asserted low by the core during transmission or if endless transmission error occurs.
TX/TXn-B	Out	Positive and negative polarity of 1553 output signals for Bus B. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-B	In	In phase and negative received signals from transceiver, Bus B
TX_INH_B	Out	Transmission inhibit signal connected to transceiver. This signal is normally high, and is asserted low by the core during transmission or if endless transmission error occurs.

4.2.2 INTERFACE TO SITAL'S DISCRETE TRANSCEIVER

When used with Sital Discrete Components Transceiver, then the channels should be connected as follows:

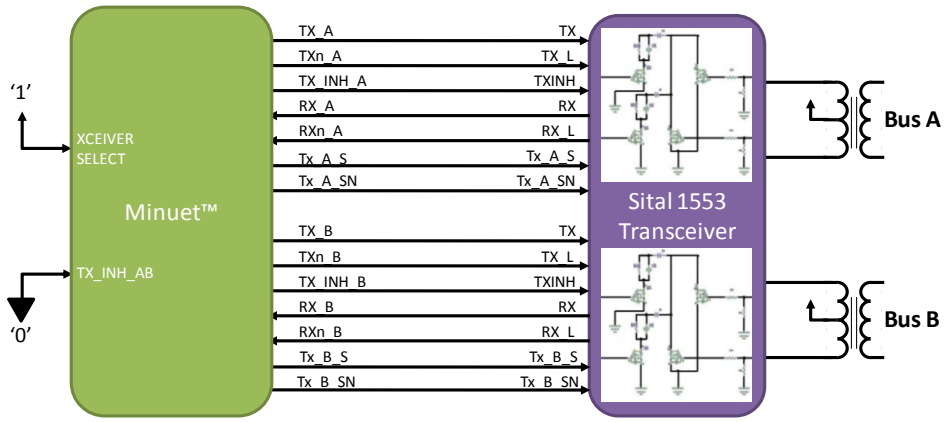


Figure 3: Interface to Sital Discrete Transceiver

Note that the Sital transceiver requires additional lines between Minuet™ and the transceivers. In addition, the line TX_INH is reversed as compared to the standard transceiver connection. Look at the Sital Transceiver documentation for further details.

The relevant pins for the Sital Discrete transceiver interface are:

Signal Name	In/Out	Description
TX_INH_AB	In	Transmitter inhibit input for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
TX/TXn-A	Out	Positive and negative polarity of 1553 output signals for Bus A. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-A	In	In phase and negative received signals from transceiver, Bus A.
TX_INH_A	Out	Transmission inhibit signal connected to transceiver. This signal is normally low, and is asserted high by the core during transmission or if endless transmission error occurs.
TX/TXn-B	Out	Positive and negative polarity of 1553 output signals for Bus B. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-B	In	In phase and negative received signals from transceiver, Bus B
TX_INH_B	Out	Transmission inhibit signal connected to transceiver. This signal is normally low, and is asserted high by the core during transmission or if endless transmission error occurs.
Tx_A_SN, **Tx_A_S,** **Tx_B_SN,** **Tx_B_S,**	Out	Connects to Sital Technology transceiver signals. Should be left unused if COTS transceiver is used

4.3 BACKEND INTERFACE – LOCAL BUS – MNT1553LB-8 AND MNT1553LB-16

Read or Write cycles with Minuet™ require data, address and control signals. Since it is assumed that Minuet™ does not necessarily uses the same clock as the host CPU, then special care is taken in order to assure data integrity.

4.3.1 LOCAL BUS PINS

Signal Name	In/Out	Description
DATA[15:0]	I/O	16 Bits DATA bus I/O.
ADDRESS[13:0]	In	14 Bits Address bus input.
MEM/REG	In	Selects between memory access and register access.
MSTCLR	In	Master Reset for Minuet. Does not reset the memory content.
CLOCK_IN	In	Clock input. Clock Range is selected by M66EN pin: • Range 1: (M66EN='0') 10, 12, 16, 20MHz or • Range 2: (M66EN='1') 24, 32 or 40MHz
READYD	Out	When non-zero wait-state mode, logic '0' on this signal indicates to the host CPU that the read or write cycle is done.
IOEN	Out	I/O Enable – This signal is low when MINUET™ is performing the requested host bus cycle. Normally this signal should not be used.
SELECT	In	Active low chip select for the MINUET™ device for memory and register access.
RD/WR	In	During Read or Write cycle to the device, when this line is logic '1' then this is a read cycle. If this line is logic '0' then data from the data bus is written to the device.
M66EN	In	Select CLOCK_IN Range, Doubles the clock frequency. For example – when clock register is set to 16MHz, then the device will work with 32MHz clock. '0' – Clock Range 1; '1' – Clock Range 2.

4.3.2 MINUET™ CLOCK INPUT

For Local-Bus interface Minuet™ can be clocked at several frequencies between 10MHz and 40MHz. The used frequency should be programmed by software into Configuration Register #6. See Software manual for details.

There are 2 ranges for input clocks, and these are determined by the input pin M66EN. If M66EN is low then the clock range is 1, and the available frequencies are 10MHz, 12MHz, 16MHz and 20MHz. if M66EN is high then the clock range is 2, and available frequencies are 20MHz, 24MHz, 32MHz and 40MHz.

The following table represents the required M66EN input and programming of Configuration Register #6 for each available clock frequency:

Input Clock Frequency	M66EN	Configuration Register #6
10MHz	0	11
12MHz	0	01
16MHz	0	00
20MHz	0	10
20MHz	1	11
24MHz	1	01
32MHz	1	00
40MHz	1	10

4.3.3 LOCAL BUS WRITE CYCLE

The following figure illustrates a write cycle. This cycle is identical between memory and registers write.

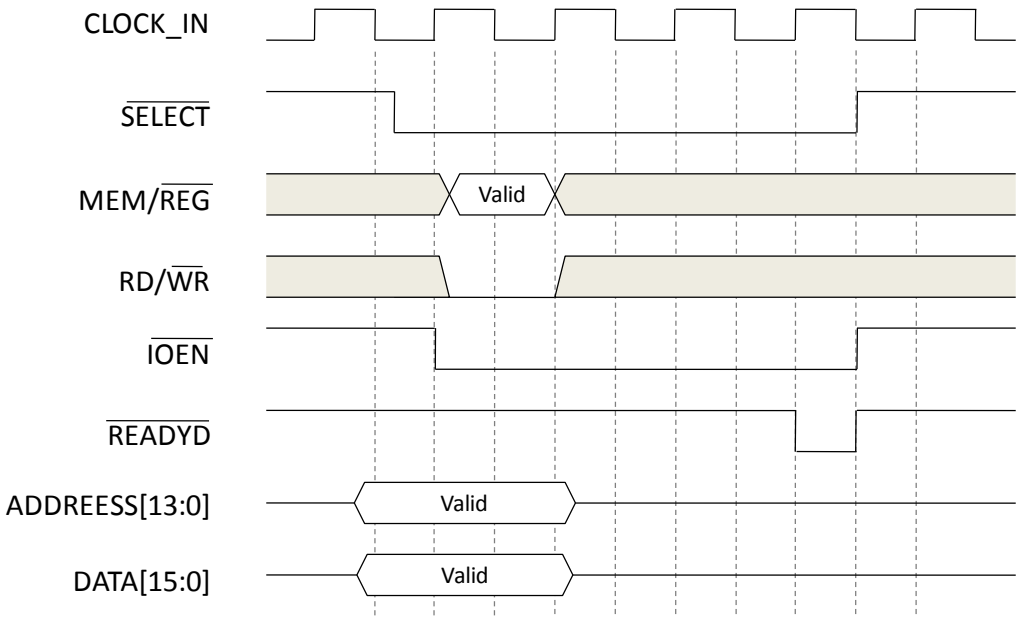


Figure 4: Local Bus Write Cycle

Notes:

1. MEM/REG is high for memory access and low for registers access.
2. MEM/REG and RD/WR are latched internally on the first falling edge of CLOCK, after SELECT is low.
3. ADDRESS is latched internally on the first rising edge after IOEN goes low.
4. DATA is latched internally on the first rising edge after IOEN goes low.

4.3.4 LOCAL BUS READ AND INTERRUPT CYCLES

The following figure illustrates a read cycle. This cycle is identical between memory and registers read.

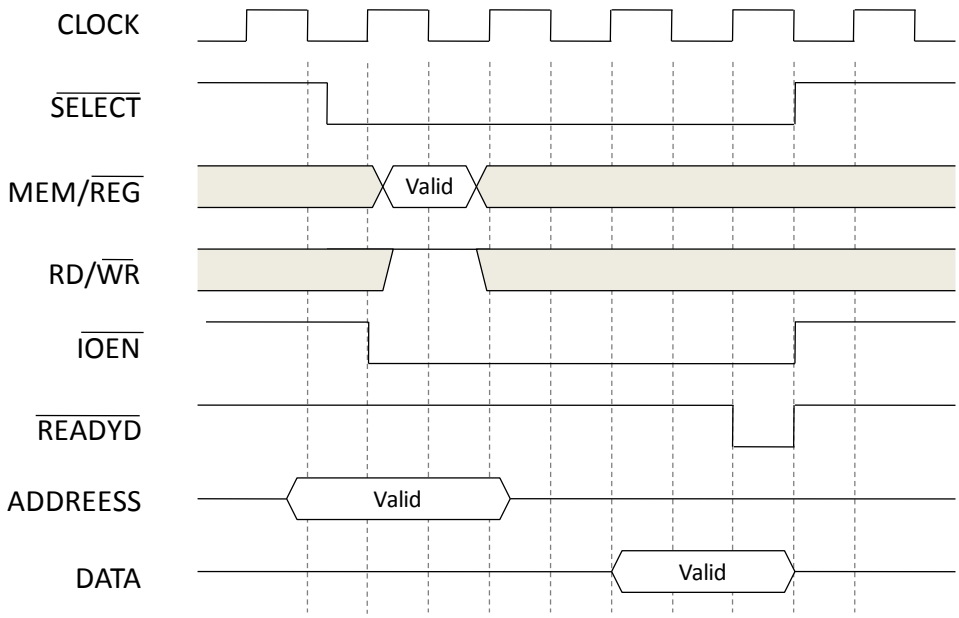


Figure 5: Local Bus Read Cycle

Notes:

1. MEM/REG is high for memory access and low for registers access.
2. MEM/REG and RD/WR are latched internally on the first falling edge of CLOCK, after SELECT is low.
3. ADDRESS is latched internally on the first rising edge after IOEN goes low.
4. Data may be valid on rising edge after ADDRESS is latched internally.

4.4 PCI BUS INTERFACE – MNT1553PCI-8 AND MNT1553PCI-16

The Minuet™ PCI interface is a standard PCI interface compliant with PCI 2.2 standard.
Vendor ID: 0x178E
Device ID: 0x2000

4.4.1 PCI PINS

The following pins are used for the PCI interface:

Signal Name	In/Out	Description
AD[31:0]:	I/O	Address and Data are multiplexed onto these pins. AD[31:0] transfers a 32-bit physical address during "address phases", and transfers 32-bits of data information during "data phases".
C/BE[3:0]#:	I/O	Bus Command and Byte Enables are multiplexed onto these pins.
PAR	I/O	Parity is even parity over the AD[31:0] and C/BE[3:0]# signals.
FRAME#	I/O	Cycle Frame is driven low by the initiator to signal the start of a new bus transaction.
TRDY#	I/O	Target Ready is driven low by the target as an indication it is ready to complete the current data phase of the transaction.
IRDY#	I/O	Initiator Ready is driven low by the initiator as an indication it is ready to complete the current data phase of the transaction.
STOP#	I/O	Stop is driven low by the target to request the initiator terminate the current transaction.
DEVSEL#	I/O	Device Select is driven active low by a PCI target when it detects its address on the PCI bus.
IDSEL	In	Initialization Device Select is used as a chip select during PCI configuration read and write transactions.
CLK	In	Clock provides the timing reference for all transfers on the PCI bus. 33/66MHz.
RST#	In	Reset is driven active low to cause a hardware reset of a PCI device
M66EN	In	Selects between 33MHz and 66MHz bus clock.
INTA#	Out	Interrupts are driven low by the device to request attention from their device driver.

5 MINUET™ PINOUT

5.1 PCI MODE – MNT1553PCI-8 AND MNT1553PCI-16[1]

	MNT1553PCI-8	MNT1553PCI-16
Signal Name	**Pin**	**Pin**
AD31	A13	
AD30	A12	
AD29	A11	
AD28	B10	
AD27	A10	
AD26	B9	
AD25	A9	
AD24	B6	
AD23	A7	
AD22	C5	
AD21	A6	
AD20	C7	
AD19	A5	
AD18	C8	
AD17	A3	
AD16	C9	
AD15	M5	
AD14	P5	
AD13	M4	
AD12	P6	
AD11	N2	
AD10	P7	
AD9	N3	
AD8	P9	
AD7	P10	
AD6	N7	
AD5	P12	
AD4	N8	
AD3	P13	
AD2	N9	
AD1	P14	
AD0	N12	
C/BE3#	A8	
C/BE2#	A2	
C/BE1#	P4	
C/BE0#	N4	
$\overline{\text{STOP}}$	M7	
$\overline{\text{IRDY}}$	A1	
$\overline{\text{TRDY}}$	M10	
$\overline{\text{PAR}}$	M6	
$\overline{\text{FRAME}}$	C10	
$\overline{\text{DEVSEL}}$	P2	
IDSEL	B3	

	MNT1553PCI-8	MNT1553PCI-16
Signal Name	**Pin**	**Pin**
$\overline{\text{INTA}}$	D13	
PCI_CLK	H14	
$\overline{\text{RESET}}$	B13	
M66EN	G3	
PCI/$\overline{\text{LB}}$	Not Applicable	
$\overline{\text{SSFLAG}}$/EXT_TRIG	D1	
BC_DISABLE	H3	
RTAD4	E1	
RTAD3	F1	
RTAD2	G1	
RTAD1	H1	
RTAD0	L1	
RT_AD_P	B2	
RT_AD_LAT	B1	
RT_BOOT	N1	
XCEIVER_SELECT	P1	
TX_INH_AB	F3	
TX-A	A14	
TXn-A	B14	
RX-A	D14	
RXn-A	E14	
TX_INH_A	F12	
TX-B	N14	
TXn-B	L14	
RX-B	G14	
RXn-B	F14	
TX_INH_B	G12	
Tx_A_SN	E12	
Tx_A_S	D12	
Tx_B_SN	H12	
Tx_B_S	J12	
VCCIO 3.3V	A4, A12, B5, B7, C3, C11, C14, F2, F13, J2, J14, K1, K12, M1, M3, M8, M9, M12, N5, N13, P1, P11	
VCC 1.2V	B11, C4, J3, J13, N11, P8	
GND	B4, B8, C1, C6, C12, C13, E2, E13, J1, M2, M11, M14, N6, N10, P3	

1. MNT1553PCI-16 pinout not determined yet.

5.2 LOCAL BUS MODE – MNT1553LB-8 AND MNT1553LB-16[1]

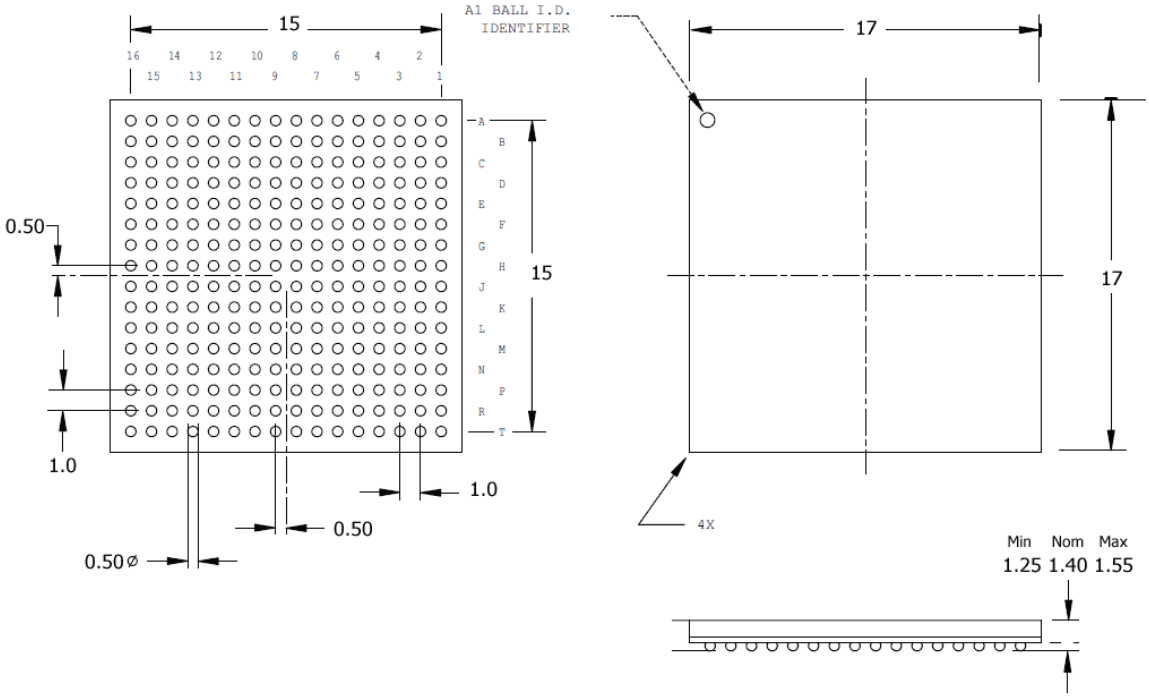
Signal Name	MNT1553LB-8 Pin	MNT1553LB-16 Pin
Data15		P6
Data14		T7
Data13		P7
Data12		T8
Data11		P8
Data10		T9
Data9		R6
Data8		T10
Data7		T11
Data6		R8
Data5		T12
Data4		R9
Data3		T13
Data2		R10
Data1		T14
Data0		R11
MEM/$\overline{REG}$		A12
Addr13		A6
Addr12		A11
Addr11		A5
Addr10		A10
Addr9		A4
Addr8		A9
Addr7		A2
Addr6		B6
Addr5		B1
Addr4		B4
Addr3		B2
Addr2		C4
Addr1		B3
Addr0		D4
$\overline{READYD}$		T5
$\overline{IOEN}$		N5
$\overline{INT}$		C1
$\overline{SELECT}$		B7
RD/$\overline{WR}$		R7
CLOCK_IN		B8
$\overline{MSTCLR}$		A13
M66EN		P10
PCI/$\overline{LB}$		D1

Signal Name	MNT1553LB-8 Pin	MNT1553LB-16 Pin
$\overline{SSFLAG}$/EXT_TRIG		F1
BC_DISABLE		G1
RTAD4		L1
RTAD3		M1
RTAD2		N1
RTAD1		P1
RTAD0		R1
RT_AD_P		K1
RT_AD_LAT		J1
RT_BOOT		H1
XCEIVER_SELECT		A14
TX_INH_AB		E1
TX-A		G16
TXn-A		H16
RX-A		F16
RXn-A		E16
TX_INH_A		D16
TX-B		P16
TXn-B		R16
RX-B		N16
RXn-B		M16
TX_INH_B		L16
Tx_A_SN		C16
Tx_A_S		B16
Tx_B_SN		J16
Tx_B_S		K16
VCCIO 3.3V		C5, C12, E3, E7, E10, E14, G5, G8, G12, H10, J7, K5, K7, K9, K12, L7, M3, M7, M10, M14, P5, P12
VCC 1.2V		G7, G9, H7, J10, K8, K10
GND		A1, A16, B5, B12, C8, E2,E15, H8, H9, H14, J3, J8, J9, M2, M15, P9, R5, R12, T1, T16

1. MNT1553LB-8 pinout not determined yet.

6 MECHANICAL DRAWINGS

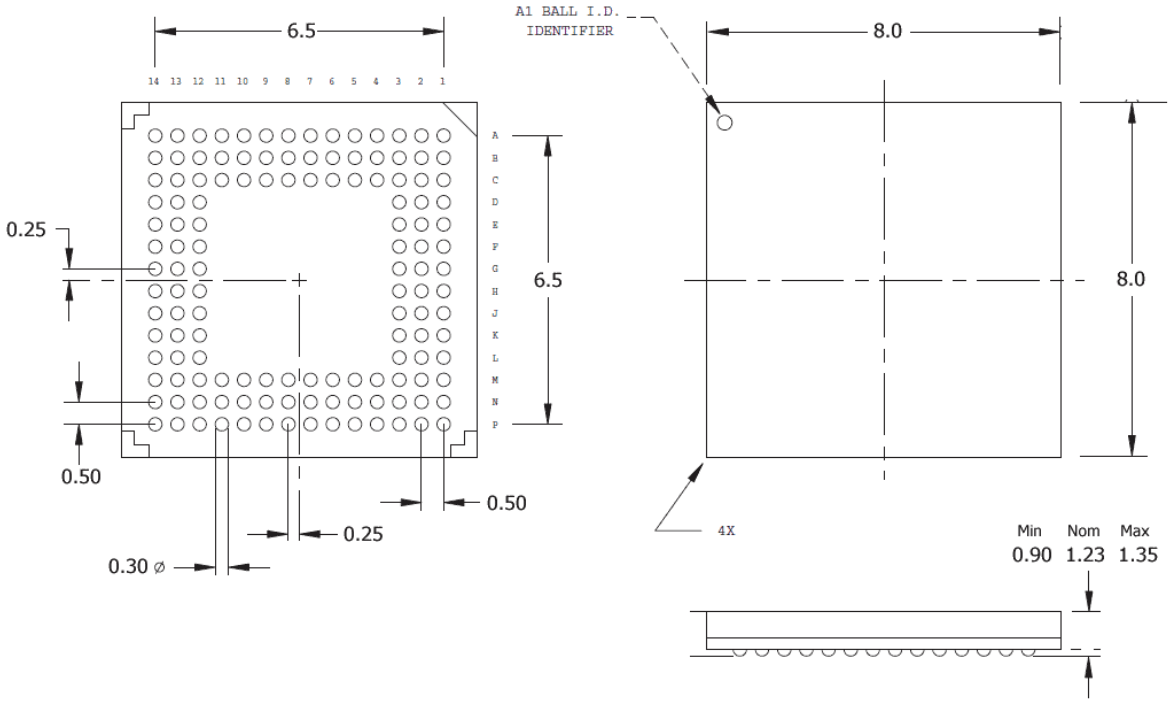
6.1 MNT1553LB-16 / MNT1553PCI-16



- All dimensions are in millimeters
- 17mm X 17mm 256-Ball ftBGA package
- 1mm pitch
- 16K Words of internal memory
- PCI or local bus interface

Figure 6: MINUET™ 17mm Package

6.2 MNT1553PCI-8 / MNT1553LB-8



- All dimensions are in millimeters
- 8mm X 8mm, 132-Ball csBGA package
- 0.5mm pitch
- 8K Words of internal memory
- PCI or local bus interface

Figure 7: MINUET™ 8mm Package

7 MINUET™ BOARD DESIGN CONSIDERATIONS

7.1 PC BOARD LAYOUT CONSIDERATIONS

7.1.1 BGA RECOMMENDATIONS

Minuet Components are packaged as BGA (Ball Grid Array) packages. Minuet-8 is arranged as fine-pitch (0.5 mm pitch) and Minuet-16 are 1mm pitch. It is important to understand how they are affected by various board layout techniques.

For specific information and layout examples, please go to
http://www.latticesemi.com/lit/docs/package/tn1074.pdf

7.1.2 POWER DECOUPLING AND BYPASS FILTERING

- Bypass capacitor usage must take into account both a low ESR as well as the self-resonant frequency.
- Vary the use of 0.1uF and 0.01µF capacitors per device power pin is a good rule of thumb.
- Locate de-coupling capacitors as close as possible to the device power pins and run short, wide traces to vias when they are required.
- Distribute some bulk capacitance (1uF and 10uF) throughout the layout to help eliminate low frequency coupling and maintain a low impedance power system.
- Use a large electrolytic capacitor (100uF) at power source.

More information available at: http://www.latticesemi.com/lit/docs/technotes/tn1068.pdf.

7.2 LOCAL BUS INTERFACE

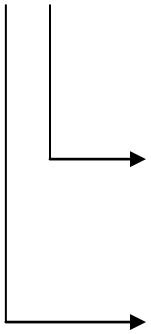
TBD

7.3 PCI INTERFACE

TBD

8 ORDERING INFORMATION

MNT1553PCI-8



Part Number	Packaging and Operating Voltage
8	8mm Package, 8K x 16 memory
16	17mm Package, 16K x 16 memory

Part Number	Product Type	Clock Freq.
PCI	PCI Interface	33/66MHz
LB	Local Bus Interface	10/12/16/20/24/32 MHz

APPENDIX A: CHANGES TRACKING

First version of this manual: 1.0

Version 1.01:

- Added details on BC_DISABLE and other inputs
- Added PCB Layout Considerations

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